Serial No. 09/239,871 TRW Docket No. 22-0071

REMARKS

The present invention is a receiver and a method of data reception. In accordance with the invention, a memory 114, including an addressable storage array, stores a sequence of data samples contained in a time division multiplexed signal, as illustrated in Fig. 3. The time division multiplexed signal is from a plurality of channels in the incoming data sequence 202. Each successive data sample belongs to a channel different from a channel to which an immediately preceding data sample belongs. The memory outputs the stored data samples in a sequence of data groups equal in number to the number of channels, which in the example of Fig. 3, is five. Each data group has a plurality of samples as illustrated in Fig. 3. The contents of the memory 114, which are read in as a sequence of data samples from different channels, are read out as a sequence of data groups, as illustrated in the bottom of Fig. 3. Thereafter a decoder, as exemplified by decoder 116 in Fig. 2, which is responsive to the sequence of data groups, decodes the data samples within the sequence of data groups and outputs the decoded data samples of the plurality of data groups from the plurality of channels.

This architecture has distinct advantages over the prior art of Fig. 1. As described in Applicant's specification with reference to Fig. 1, the prior art hardware identified by reference numeral 10 requires replication for each channel.

In contrast, the present invention has an exemplary architecture illustrated in Fig. 2 that utilizes only a single memory 114 and an inner decoder 116 to achieve decoding of data for the R channels of Fig. 1. The present invention requires substantially less hardware requirements than the prior art. See Applicant's specification, beginning on

page 17, line 9, for a discussion regarding the hardware reduction achieved by the present invention.

Claims 1, 13 and 17 stand rejected under 35 U.S.C. §102(b) as being anticipated by United States Patent 5,448,592 (Williams et al.). Specifically, the Examiner reasons as follows:

6. Regarding claim 1, Williams et al. shows a receiver comprising: a memory (Williams fig. 10: 7, 8, 9) including an addressable storage array which stores a sequence of data samples contained in a time division multiplexed signal (Williams et al. claim 13; col. 15 lines 8 to 23 as shown by the applicant) from a plurality of channels (Williams fig. 10: 32 bit inputs into 7 through 9) with each successive data sample (Williams fig. 10: LSB then output of 8 then MSB) belonging to a channel different from a channel to which an immediately preceding data sample belongs (Williams fig. 10: LSB, output of 8 and MSB are all from different shift register channels) and outputs the stored data samples in a sequence of data groups (Williams fig. 10: LSB is data group which can mean only one bit; similarly output of 8 is another group and MSB is another group) equal in number to the number of the plurality of channels (Williams fig. 10: three shift register channels 7, 8 and 9 and 3 data groups LSB, output of 8 and MSB) with each data group containing a plurality of samples from one of the plurality of channels; and a decoder (Williams fig. 10: 13 modulator which decodes the bits into a modulated signal), responsive to the sequence of data groups, which decodes the data samples within the data groups and outputs decoded data samples of the plurality of data groups from the plurality of channels (Williams fig. 10; 13 is outputting the decoded data samples of the plurality of data groups from the plurality of channels).

3. The discussion of claim 1 applies to claim 17.

4. Regarding claim 13, it is inherent for the memory in Williams et al. to comprise a write address generator and a read address generator and the addressable storage array contains memory cells which are addressed by addresses generated by the write address generator and the read address generator, the sequence of data samples being written in a group of memory cells with addresses generated by the write address generator, and the sequence of data groups being read out with addresses generated by the read address generator. It is inherent since these are characteristic elements of a memory.

These grounds of rejection are traversed for the following reasons. The Examiner has now switched his interpretation of Williams et al. as Fig. 10 anticipating the claims in place of Fig. 11 anticipating the claims. At the outset, it should be noted that Fig. 10 is a coder (transmitter), whereas independent claims 1 and 17 recite a receiver and a method of data reception. As the Examiner is aware, for an anticipated rejection to be proper, every element of the claimed invention must be shown in the part of the reference that is relied upon which, in this case, is a coder (transmitter). A coder cannot be read upon a receiver or a method of data reception when the preambles of independent claims 1 and 17 are given weight.

Moreover, the Examiner again relies upon claim 13 of Williams et al. for the teaching of a time division multiplexed signal in Fig. 10 as recited in independent claims 1 and 17. Specifically, claim 13 of Williams et al. recites "time division multiplex means, synchronized to the block timing means, for confined data input to the apparatus and additional information to produce the block of bits to be transmitted." This subject matter, as may be seen by the reference to "the block of bits to be transmitted" covers a coder instead of a receiver and a method of data reception.

It should be further noted that the "time multiplexed means" of claim 13 reads upon the decoder shown in Fig. 18 which is described, beginning in column 14, lines 32 et seq. through column 15, line 45. The aforementioned portions of columns 14 and 15 pertain to the embodiment illustrated in Fig. 18 which is a decoder unrelated to the coder of Fig. 10. Moreover, the coder of Fig. 17, which is associated with the decoder of Fig. 18, has a different architecture than the coder of Fig. 10.

The Examiner's reliance upon Fig. 10 of Williams et al. as anticipating claims 1, 13, and 18 would not even be considered by a person of ordinary skill in the art as relating to the decoder of Fig. 18. It is submitted that the Examiner's interpretation of Williams et al., which relies upon Fig. 10 as anticipating, is incompatible with reliance upon claim 13 for the claimed time multiplexed signal upon which Fig. 18 is readable.

Williams et al. discloses in Fig. 10, a coder that produces output signal 16 that is demodulated by demodulator 20 of Fig. 11. In Fig. 10, an input 1, which is data, is clocked into a sixty-four bit serial to parallel shift register 2. Every sixty-four bits of the input data are output as a parallel sixty-four-bit word into register 4. From register 4, six bits are fed to coder 5 and twenty-six bits are fed to coder 6. Coder 5 implements a (32, 6, 16) Reed-Muller decoder and produces thirty-two bits a_{1j} and coder 6 is an (32, 26, 4) extended Hamming-coder that produces thirty-two bits a_{2j}. A remaining thirty-two bits a_{3j} are produced in an uncoded form, as shown in Fig. 9. See column 7, lines 31-50.

The ninety-six bits comprising a_{1j}, a_{2j}, and a_{3j} are fed to registers 7-12. See column 7, lines 51-63. The contents of the registers 7-12 are X and Y coordinates of sixteen symbols to be transmitted. A three-bit word representing the X coordinate of the symbol to be transmitted is output by registers 7-9 and a three bit data word representing the Y coordinates is output by registers 10-12. See column 7, lines 63 through column 8, line 5.

The outputs from the registers 7-9 and 10-12 respectively modulate orthogonal carriers C_I and C_Q which are summed together in the output 16. See column 8, lines 6-19.

It is clearly seen from the foregoing explanation of Fig. 10, upon which the Examiner relies, that a person of ordinary skill in the art would not consider Williams et al. to disclose the claimed time division multiplexed signal recited in independent claims 1 and 17. It is apparent that the Examiner is attempting to stretch Fig. 10 of Willliams et al., which discloses a code to include the decoder of Fig. 18.

Since the Examiner has the burden of proof on anticipation to show that every element of a claim is disclosed in the portion of Williams relied upon, it is incumbent upon the Examiner to demonstrate how the coder of Fig. 10 of Williams et al. can be interpreted to include time division multiplexed signals which are only disclosed in the decoder of Fig. 18 of Williams. Such a reading of Williams et al. is erroneous and cannot be the basis for an anticipation rejection.

Claims 2-12, 14-16 and 18-29 stand rejected as being obvious over Williams et al. The Examiner's statement of the rejection regarding obviousness does not cure the deficiencies noted above with respect to Williams et al.

Moreover, it seems that the Examiner has improperly included a reference to Linsky in paragraph 12 of the Final Rejection that is part of the obviousness rejection over Williams et al. Clarification on the record is requested.

In any event, it is noted that the Examiner in the initial portion of the Office action discusses Applicant's prior argument regarding Linsky in paragraph 3. It is submitted that a channelizer as the Examiner has interpreted as being only a signal path does not meet claims 9-12. Claims 9-12 recite "a channelizer, which is responsive to an input bandwidth which divides the input bandwidth into a plurality of output channels each of

equal bandwidth, one of the output channels comprising the time division multiplexed signal" which cannot be met by a mere path for signals.

With respect to the overall rejection regarding obviousness, it is submitted that the only basis for making a modification of Williams et al. to meet the claimed subject matter would be based upon impermissible hindsight. The Examiner's statement in Section 4 of the Office action that a conclusion of obviousness "is in a sense necessarily a reconstruction based upon hindsight reasoning" is a misstatement of the law. Hindsight reasoning is not part of a proper determination of whether subject matter is obvious under Section 103.

In view of the foregoing remarks, it is submitted that the claims in the application are in condition for allowance. Accordingly, early allowance thereof is respectfully requested.

Respectfully submitted,

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Noel F. Heal
Registration Number 26,074

TRW INC.
Intellectual Asset Management
One Space Park, E2/6072
Redondo Beach, CA 90278
Telephone: (310) 812-4910
FAX: (310) 812-2687